INTEGRATED CIRCUITS

DATA SHEET

TEA6324T
Sound control circuit

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors





FEATURES

- Source selector for two stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume and balance control
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Fast mute control via I^2C-bus
- Fast mute control via pin
- I^2C-bus control for all functions
- Power supply with internal power-on reset.



GENERAL DESCRIPTION

The sound control circuit TEA6324T is an I^2C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–18	–	+18	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6324T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

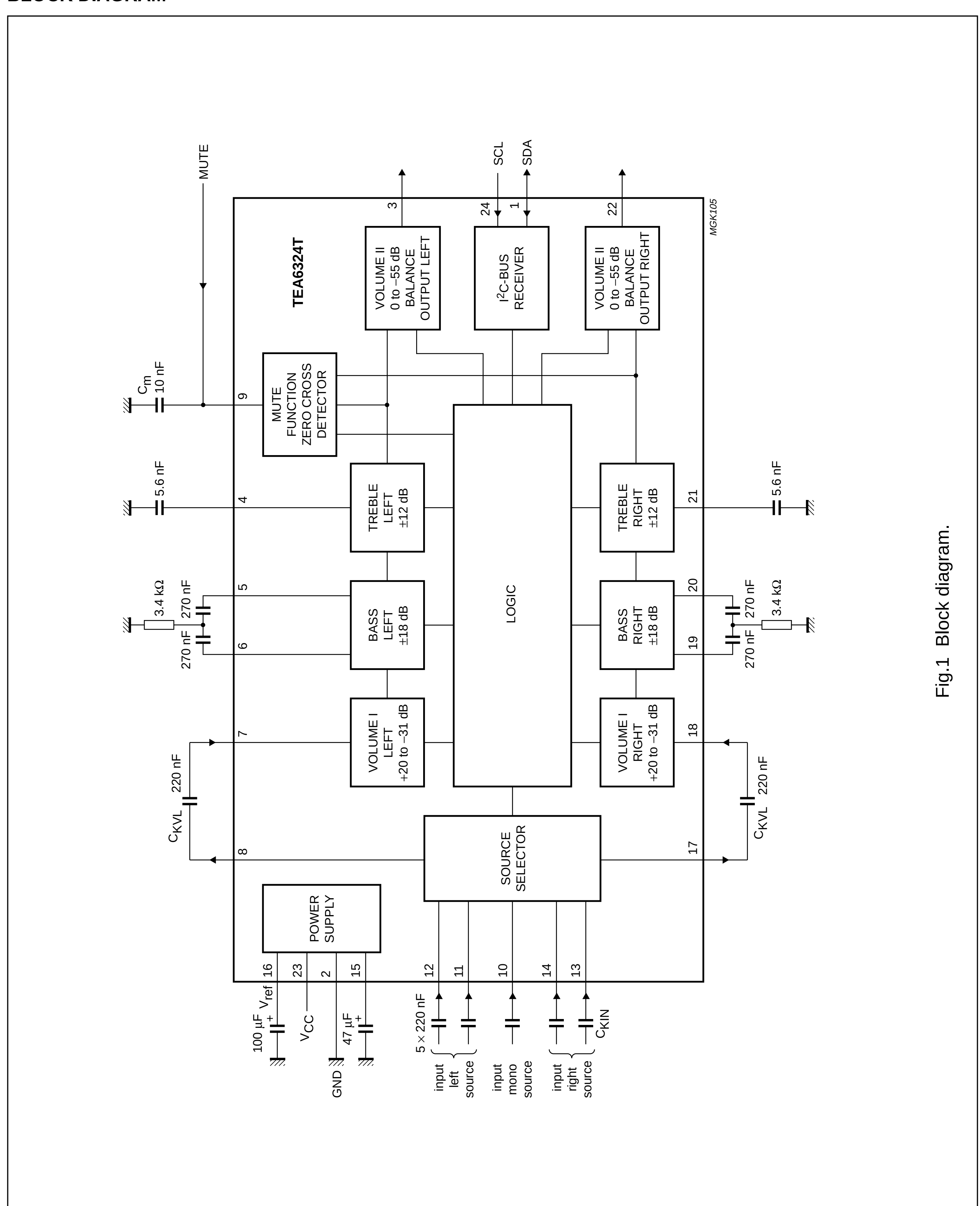


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output (I^2C-bus)
GND	2	ground
OUTL	3	output left
TL	4	treble control capacitor left channel or input from an external equalizer
B2L	5	bass control left channel or output to an external equalizer
B1L	6	bass control, left channel
IVL	7	input volume I, left control part
QSL	8	output source selector, left channel
MUTE	9	mute control
IMO	10	input mono source
IBL	11	input B left source
IAL	12	input A left source
IAR	13	input A right source
IBR	14	input B right source
CAP	15	electronic filtering for supply
V_{ref}	16	reference voltage ($0.5V_{CC}$)
QSR	17	output source selector right channel
IVR	18	input volume I, right control part
B1R	19	bass control right channel
B2R	20	bass control right channel or output to an external equalizer
TR	21	treble control capacitor right channel or input from an external equalizer
OUTR	22	output right
V_{CC}	23	supply voltage
SCL	24	serial clock input (I^2C-bus)

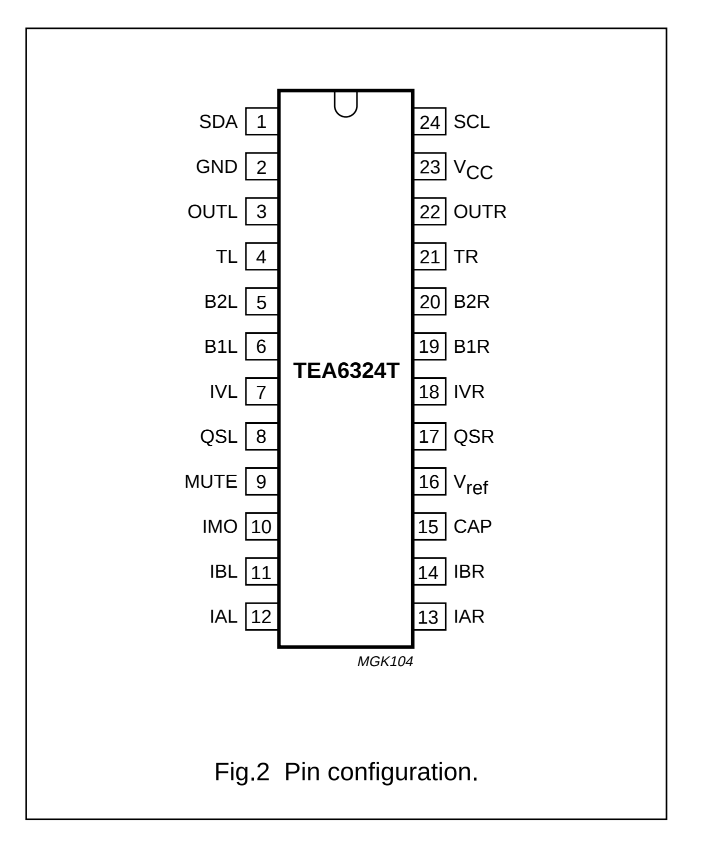


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 2 stereo inputs or the mono input. The maximum input signal voltage is $V_{i(rms)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 7 and 8 for the left channel and pins 17 and 18 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and –31 dB in steps of 1 dB. The volume II control range is between 0 dB and –55 dB in steps of 1 dB.
The recommended control range to be used is 86 dB (+20 to –66 dB) although in theory, a range of 106 dB (+20 to –86 dB) can be attained. The gain/attenuation setting of the volume I control block is common for both channels.

The volume I control block is followed by the bass control block. The frequency response of the bass control (see Fig.3) is provided for each channel by an external filter in combination with internal resistors. The adjustable range is between –18 and +18 dB in steps of 1.8 dB at 46 Hz.

The treble control block offers a control range between –12 and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of treble control is 3 dB.
The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I^2C-bus. In this event the internal signal flow is disconnected. The connections B2L and B2R are outputs and TL and TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block.
The balance function uses the same control block. This is achieved by 2 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes:

1. Zero crossing mode mute via I^2C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 8 and Fig.15)
2. Fast mute via MUTE pin (see Fig.9)
3. Fast mute via I^2C-bus either by general mute (GMU, see Tables 2 and 8) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. Two comparators are built-in to provide independent mute switches to control each of the audio channels (left and right).

To avoid a large delay of mute switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.9). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit, only if no zero crossing was detected during that time.

The mute function can also be controlled externally (see Fig.9). If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I^2C-bus for the time the pin is held LOW. The hardware mute position is not stored in the TEA6324T.

Typically, the turn on/off can be used to avoid AF output. This can be caused by the input signal from preceding stages, which may produce output during a drop of V_{CC}. To avoid this, the mute must be set prior to a V_{CC} drop and can be achieved either by I^2C-bus control, or by grounding the MUTE pin.

In cases where there is no mute in the application before turn off, a supply voltage drop of more than $1 \times V_{BE}$ will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after a certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is ideal for use in Radio Data System (RDS) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e.g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_n	voltage at all pins relative to pin 2		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 1	–	–	

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV. Machine model: C = 200 pF; R = 0 Ω; V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC coupled; f = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; bass linear; treble linear; balance in mid position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 16		–	4.25	–	V
$G_{v(max)}$	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(rms)}$	output voltage level (RMS value) for					
	P_{max} at the power output stage	THD ≤ 0.1%; see Fig.10	–	2000	–	mV
	start of clipping	THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
f_{ro}	roll-off frequency	C_{KIN} = 220 nF; C_{KVL} = 220 nF; Z_i = $Z_{i(min)}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; Z_i = $Z_{i(typ)}$ low frequency (–3 dB)	17	–	–	Hz
α_{cs}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1 V; G_v = 0 dB	–	0.05	0.15	%
		V_i = 2 V; G_v = 0 dB	–	0.1	–	%
		V_i = 2 V; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(rms)}$ < 200 mV				
		f = 100 Hz	70	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz RMS; V_o = 2.0 V; see Figs 5 and 6	–	105	–	dB
		CCIR468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(rms)}$	noise output power (RMS value) only contribution of TEA6324T; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_{ct}	crosstalk between bus inputs and signal outputs $\left(20\ \log\frac{V_{bus(p-p)}}{V_{o(rms)}}\right)$	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
V_{offset}	DC offset voltage at source selector output by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
R_{DCL}	DC load resistance at output to ground		4.7	–	–	kΩ
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
$V_{n(o)}$	noise output voltage	CCIR468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
CR_{tot}	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
α_{mute}	mute attenuation	see Fig.9	100	110	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{offset}	DC step offset between any adjoining step	G_v = 0 to –66 dB	–	0.2	10	mV
		G_v = 20 to 0 dB	–	2	15	mV
	DC step offset between any step to mute	G_v = 0 to –66 dB	–	–	10	mV
Volume I control						
$CR_{tot(vol)1}$	continuous volume control range		–	51	–	dB
G_v	voltage gain		–31	–	+20	dB
G_{step}	step resolution		–	1	–	dB
Bass control						
G_{bass}	bass control, maximum boost	f = 46 Hz	16	18	19	dB
	maximum attenuation	f = 46 Hz	16	18	19	dB
G_{step}	step resolution (toggle switching)	f = 46 Hz	–	1.8	–	dB
	step error between any adjoining step	f = 46 Hz	–	–	0.5	dB
V_{offset}	DC step offset in any bass position		–	–	25	mV
Treble control						
G_{treble}	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
V_{offset}	DC step offset in any treble position		–	–	10	mV
Volume II and balance control						
$CR_{tot(vol)2}$	continuous attenuation of volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function (see Fig.9)						
HARDWARE MUTE						
V_{sw}	mute switch level (2 × V_{BE})		–	1.45	–	V
mute active						
V_{swLOW}	input level		–	–	1.0	V
I_i	input current	V_{swLOW} = 1 V	–300	–	–	µA
mute passive: level internally defined						
V_{swHIGH}	saturation voltage		–	–	V_{CC}	V
$t_{d(mute)}$	delay until mute passive		–	–	0.5	ms
ZERO CROSSING MUTE						
I_{dch}	discharge current		0.3	0.6	1.2	µA
I_{ch}	charge current		–300	–150	–	µA
V_{swDEL}	delay switch level (3 × V_{BE})		–	2.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_d	delay time	C_m = 10 nF	–	100	–	ms
$V_{(w)}$	window for audio signal zero crossing detection		–	30	40	mV
Muting at power supply drop						
V_{CCdrop}	supply drop for mute active		–	V_{23} – 0.7	–	V
Power-on reset when reset is active the GMU-bit (general mute) is set and the I^2C-bus receiver is in reset position						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.5	7.2	V
	decreasing supply voltage start of reset		4.2	5.5	6.2	V
Digital part (I^2C-bus pins); note 3						
V_{IH}	HIGH-level input voltage		3	–	9.5	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	μA
I_{IL}	LOW-level input current		–10	–	+10	μA
V_{OL}	LOW-level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V (p-p).
3. The AC characteristics are in accordance with the I^2C-bus specification. This specification, *“The I^2C-bus and how to use it”*, can be ordered using the code 9398 393 40011.

I^{2}C-BUS PROTOCOL

I^{2}C-bus format

S(1)	SLAVE ADDRESS(2)	A(3)	SUBADDRESS(4)	A(3)	DATA(5)	A(3)	P(6)

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 0101 0000.
3. A = acknowledge, generated by the slave.
4. SUBADDRESS (SAD), see Table 1.
5. DATA, see Table 1.
6. P = STOP condition.

Table 1 Second byte after MAD

FUNCTION	BIT	MSB							LSB
		7	**6**	**5**	**4**	**3**	**2(1)**	**1(1)**	**0(1)**
Volume	V	0	0	0	0	0	0	0	0
Output right	OUTR	0	0	0	0	0	0	0	1
Output left	OUTL	0	0	0	0	0	0	1	0
No function	–	0	0	0	0	0	0	1	1
No function	–	0	0	0	0	0	1	0	0
Bass	BA	0	0	0	0	0	1	0	1
Treble	TR	0	0	0	0	0	1	1	0
Switch	S	0	0	0	0	0	1	1	1

Note

1. Significant subaddress.

Table 2 Definition of third byte after MAD and SAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2	1	0
Volume	V	ZCM(1)	1	V5(2)	V4(2)	V3(2)	V2(2)	V1(2)	V0(2)
Output right	OUTR	X(3)	X(3)	OUTR5(4)	OUTR4(4)	OUTR3(4)	OUTR2(4)	OUTR1(4)	OUTR0(4)
Output left	OUTL	X(3)	X(3)	OUTL5(5)	OUTL4(5)	OUTL3(5)	OUTL2(5)	OUTL1(5)	OUTL0(5)
No function	–	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)
No function	–	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)
Bass	BA	X(3)	X(3)	X(3)	BA4(6)	BA3(6)	BA2(6)	BA1(6)	BA0(6)
Treble	TR	X(3)	X(3)	X(3)	TR4(7)	TR3(7)	TR2(7)	TR1(7)	TR0(7)
Switch	S	GMU(8)	X(3)	X(3)	X(3)	X(3)	SC2(9)	SC1(9)	SC0(9)

Notes

1. Zero crossing mode.
2. Volume control.
3. Don’t care bits (logic 1 during testing).
4. Output right.
5. Output left.
6. Bass control.
7. Treble control.
8. Mute control for all outputs (general mute).
9. Source selector control.

Table 3 Volume I setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
+20	1	1	1	1	1	1
+19	1	1	1	1	1	0
+18	1	1	1	1	0	1
+17	1	1	1	1	0	0
+16	1	1	1	0	1	1
+15	1	1	1	0	1	0
+14	1	1	1	0	0	1
+13	1	1	1	0	0	0
+12	1	1	0	1	1	1
+11	1	1	0	1	1	0
+10	1	1	0	1	0	1
+9	1	1	0	1	0	0
+8	1	1	0	0	1	1
+7	1	1	0	0	1	0
+6	1	1	0	0	0	1
+5	1	1	0	0	0	0
+4	1	0	1	1	1	1
+3	1	0	1	1	1	0
+2	1	0	1	1	0	1
+1	1	0	1	1	0	0
0	1	0	1	0	1	1
–1	1	0	1	0	1	0
–2	1	0	1	0	0	1
–3	1	0	1	0	0	0
–4	1	0	0	1	1	1
–5	1	0	0	1	1	0
–6	1	0	0	1	0	1
–7	1	0	0	1	0	0
–8	1	0	0	0	1	1
–9	1	0	0	0	1	0
–10	1	0	0	0	0	1
–11	1	0	0	0	0	0
–12	0	1	1	1	1	1
–13	0	1	1	1	1	0
–14	0	1	1	1	0	1
–15	0	1	1	1	0	0
–16	0	1	1	0	1	1
–17	0	1	1	0	1	0

G_v (dB)	DATA					
	V5	**V4**	**V3**	**V2**	**V1**	**V0**
–18	0	1	1	0	0	1
–19	0	1	1	0	0	0
–20	0	1	0	1	1	1
–21	0	1	0	1	1	0
–22	0	1	0	1	0	1
–23	0	1	0	1	0	0
–24	0	1	0	0	1	1
–25	0	1	0	0	1	0
–26	0	1	0	0	0	1
–27	0	1	0	0	0	0
–28	0	0	1	1	1	1
–29	0	0	1	1	1	0
–30	0	0	1	1	0	1
–31	0	0	1	1	0	0
Repetition of steps in a range from –28 dB to –31 dB						
–28	0	0	1	0	1	1
–29	0	0	1	0	1	0
–30	0	0	1	0	0	1
–31	0	0	1	0	0	0
–28	0	0	0	1	1	1
–29	0	0	0	1	1	0
–30	0	0	0	1	0	1
–31	0	0	0	1	0	0
–28	0	0	0	0	1	1
–29	0	0	0	0	1	0
–30	0	0	0	0	0	1
–31	0	0	0	0	0	0

Table 4 Volume II setting; note 1

G_v (dB)	DATA					
	OUTL5	OUTL4	OUTL3	OUTL2	OUTL1	OUTL0
	OUTR5	OUTR4	OUTR3	OUTR2	OUTR1	OUTR0
0	1	1	1	1	1	1
–1	1	1	1	1	1	0
–2	1	1	1	1	0	1
–3	1	1	1	1	0	0
–4	1	1	1	0	1	1
–5	1	1	1	0	1	0
–6	1	1	1	0	0	1
–7	1	1	1	0	0	0
–8	1	1	0	1	1	1
–9	1	1	0	1	1	0
–10	1	1	0	1	0	1
–11	1	1	0	1	0	0
–12	1	1	0	0	1	1
–13	1	1	0	0	1	0
–14	1	1	0	0	0	1
–15	1	1	0	0	0	0
–16	1	0	1	1	1	1
–17	1	0	1	1	1	0
–18	1	0	1	1	0	1
–19	1	0	1	1	0	0
–20	1	0	1	0	1	1
–21	1	0	1	0	1	0
–22	1	0	1	0	0	1
–23	1	0	1	0	0	0
–24	1	0	0	1	1	1
–25	1	0	0	1	1	0
–26	1	0	0	1	0	1
–27	1	0	0	1	0	0
–28	1	0	0	0	1	1
–29	1	0	0	0	1	0
–30	1	0	0	0	0	1
–31	1	0	0	0	0	0
–32	0	1	1	1	1	1
–33	0	1	1	1	1	0
–34	0	1	1	1	0	1
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1

G_v (dB)	DATA					
	OUTL5	OUTL4	OUTL3	OUTL2	OUTL1	OUTL0
	OUTR5	OUTR4	OUTR3	OUTR2	OUTR1	OUTR0
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
Mute	0	0	0	1	1	1
Mute	0	0	0	1	1	0
Mute	0	0	0	1	0	1
Mute	0	0	0	1	0	0
Mute	0	0	0	0	1	1
Mute	0	0	0	0	1	0
Mute	0	0	0	0	0	1
Mute	0	0	0	0	0	0

Note

1. For a particular range the data is always the same, only the subaddress changes.

Table 5 Bass setting

G_{bass} (dB)	DATA				
	BA4	**BA3**	**BA2**	**BA1**	**BA0**
+18.0	1	1	1	1	1
+16.2	1	1	1	1	0
+18.0	1	1	1	0	1
+16.2	1	1	1	0	0
+18.0	1	1	0	1	1
+16.2	1	1	0	1	0
+14.4	1	1	0	0	1
+12.6	1	1	0	0	0
+10.8	1	0	1	1	1
+9.0	1	0	1	1	0
+7.2	1	0	1	0	1
+5.4	1	0	1	0	0
+3.6	1	0	0	1	1
+1.8	1	0	0	1	0
0(1)	1	0	0	0	1
0(2)	1	0	0	0	0
–1.8	0	1	1	1	1
–3.6	0	1	1	1	0
–5.4	0	1	1	0	1
–7.2	0	1	1	0	0
–9.0	0	1	0	1	1
–10.8	0	1	0	1	0
–12.6	0	1	0	0	1
–14.4	0	1	0	0	0
–16.2	0	0	1	1	1
–18.0	0	0	1	1	0
–16.2	0	0	1	0	1
–18.0	0	0	1	0	0
Note 3	0	0	0	1	1
Note 3	0	0	0	1	0
Note 3	0	0	0	0	1
Notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.8 dB boost and 1.8 dB attenuation.
3. The last four bass control data words mute the bass response.
4. The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_{treble} (dB)	DATA				
	TR4	**TR3**	**TR2**	**TR1**	**TR0**
+12.0	1	1	1	1	1
+10.5	1	1	1	1	0
+12.0	1	1	1	0	1
+10.5	1	1	1	0	0
+12.0	1	1	0	1	1
+10.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0(1)	1	0	0	0	1
0(2)	1	0	0	0	0
–1.5	0	1	1	1	1
–3.0	0	1	1	1	0
–4.5	0	1	1	0	1
–6.0	0	1	1	0	0
–7.5	0	1	0	1	1
–9.0	0	1	0	1	0
–10.5	0	1	0	0	1
–12.0	0	1	0	0	0
Note 3	0	0	1	1	1
Note 3	0	0	1	1	0
Note 3	0	0	1	0	1
Note 3	0	0	1	0	0
Note 3	0	0	0	1	1
Note 3	0	0	0	1	0
Note 3	0	0	0	0	1
Notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last eight treble control data words select treble output.
4. The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Selected input

FUNCTION	DATA		
	SC2	SC1	SC0
Stereo inputs IAL and IAR	1	1	1
Stereo inputs IBL and IBR	1	1	0
No function	1	0	1
No function	1	0	0
Mono input IMO	0	X[(1)]	X[(1)]

Note

1. X = don’t care bits (logic 1 during testing).

Table 8 Mute mode

FUNCTION	DATA	
	GMU	ZCM
Direct mute off	0	0
Mute off delayed until the next zero crossing	0	1
Direct mute	1	0
Mute delayed until the next zero crossing	1	1

MED840

G_{bass} (dB)

20, 10, 0, −10, −20

10, 10^2, 10^3, f (Hz), 10^4

Fig.3 Bass control.

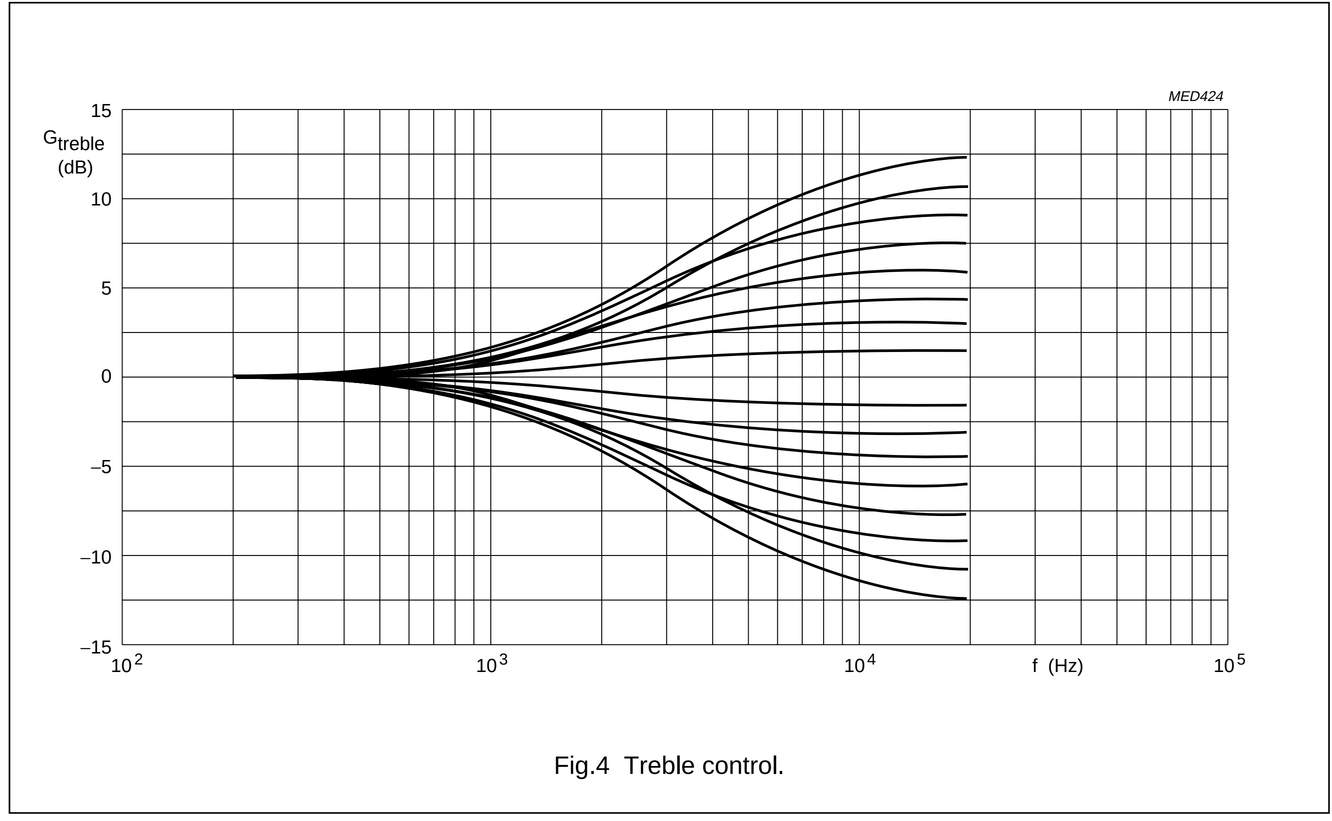


Fig.4 Treble control.

MED426

S/N (dB)

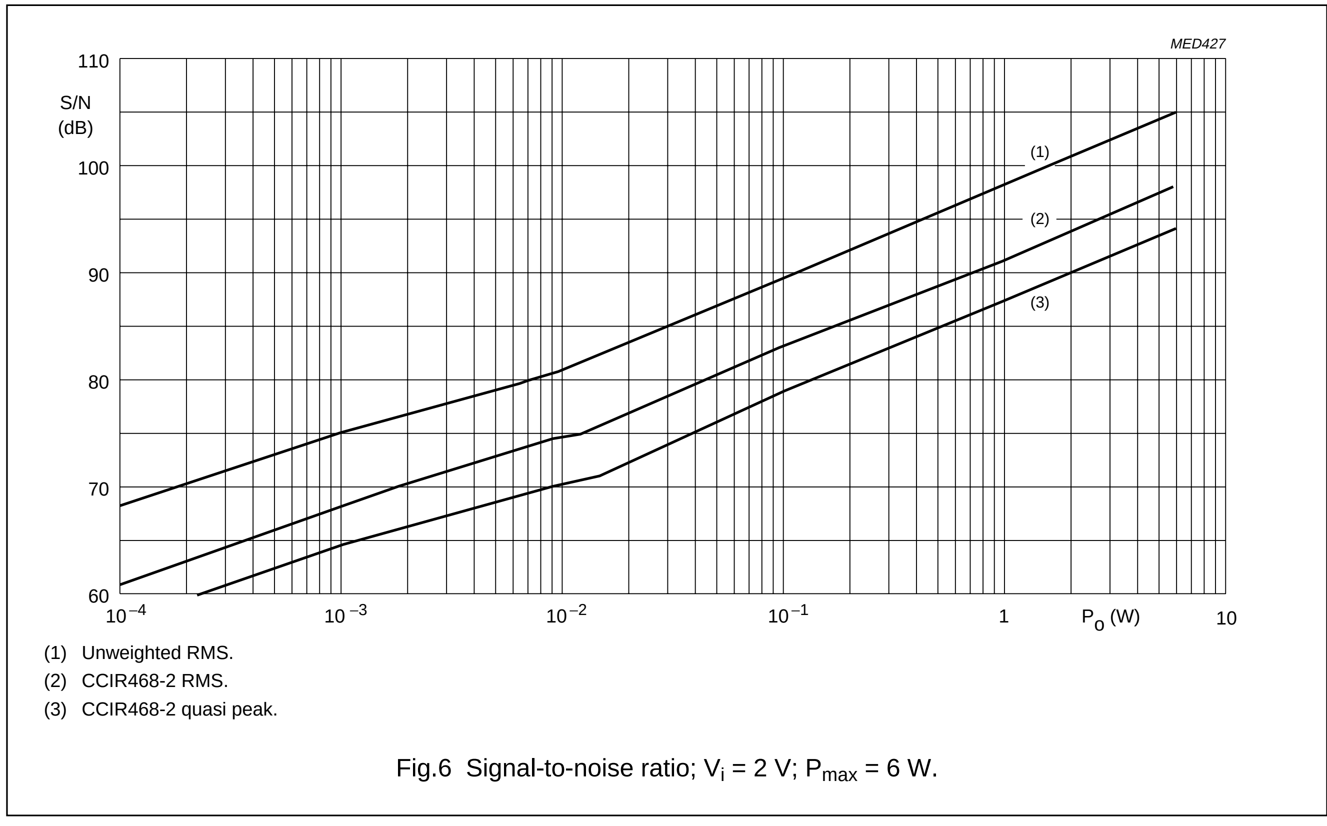
100
90
80
70
60
50

10^{-4} 10^{-3} 10^{-2} 10^{-1} 1 P_o (W) 10

(1)
(2)
(3)

(1) V_i = 2.0 V.
(2) V_i = 0.5 V.
(3) V_i = 0.2 V.

Fig.5 Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.



(1) Unweighted RMS.
(2) CCIR468-2 RMS.
(3) CCIR468-2 quasi peak.

Fig.6 Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.

MHA594

noise (μV)

200

150

100

50

0

–70 –50 –30 –10 10 30

gain (dB)

Stereo/mono inputs.

Fig.7 Noise output voltage; CCIR468-2, quasi peak.

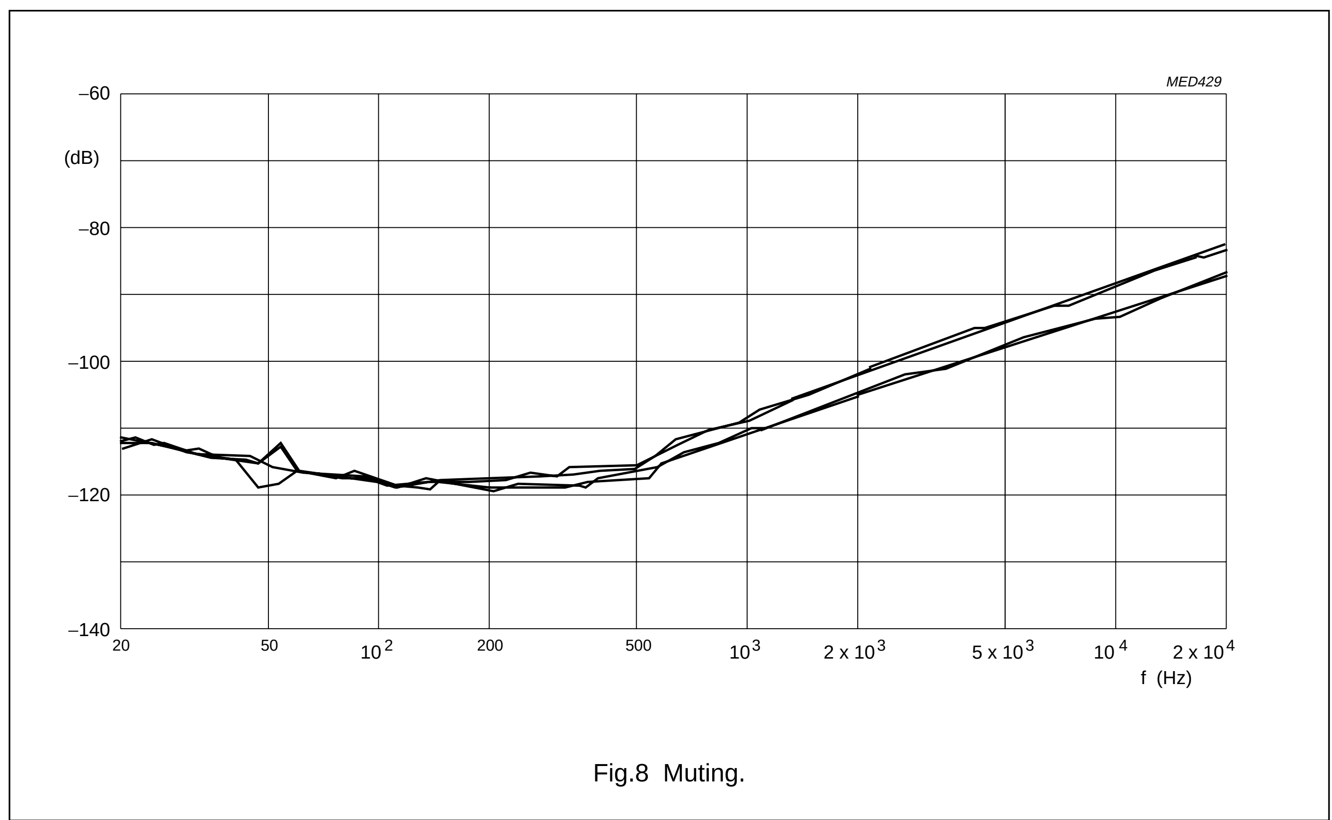
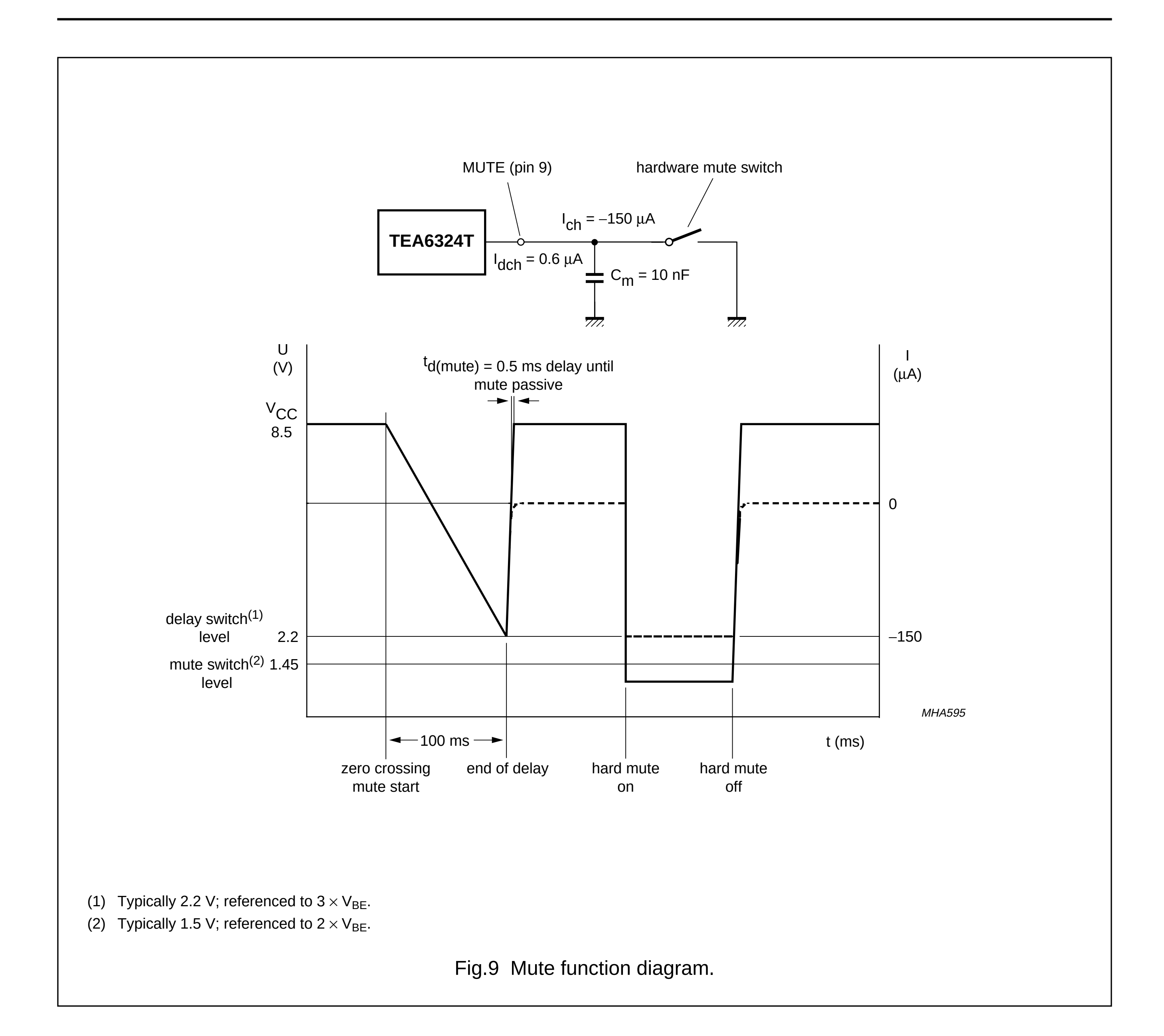


Fig.8 Muting.

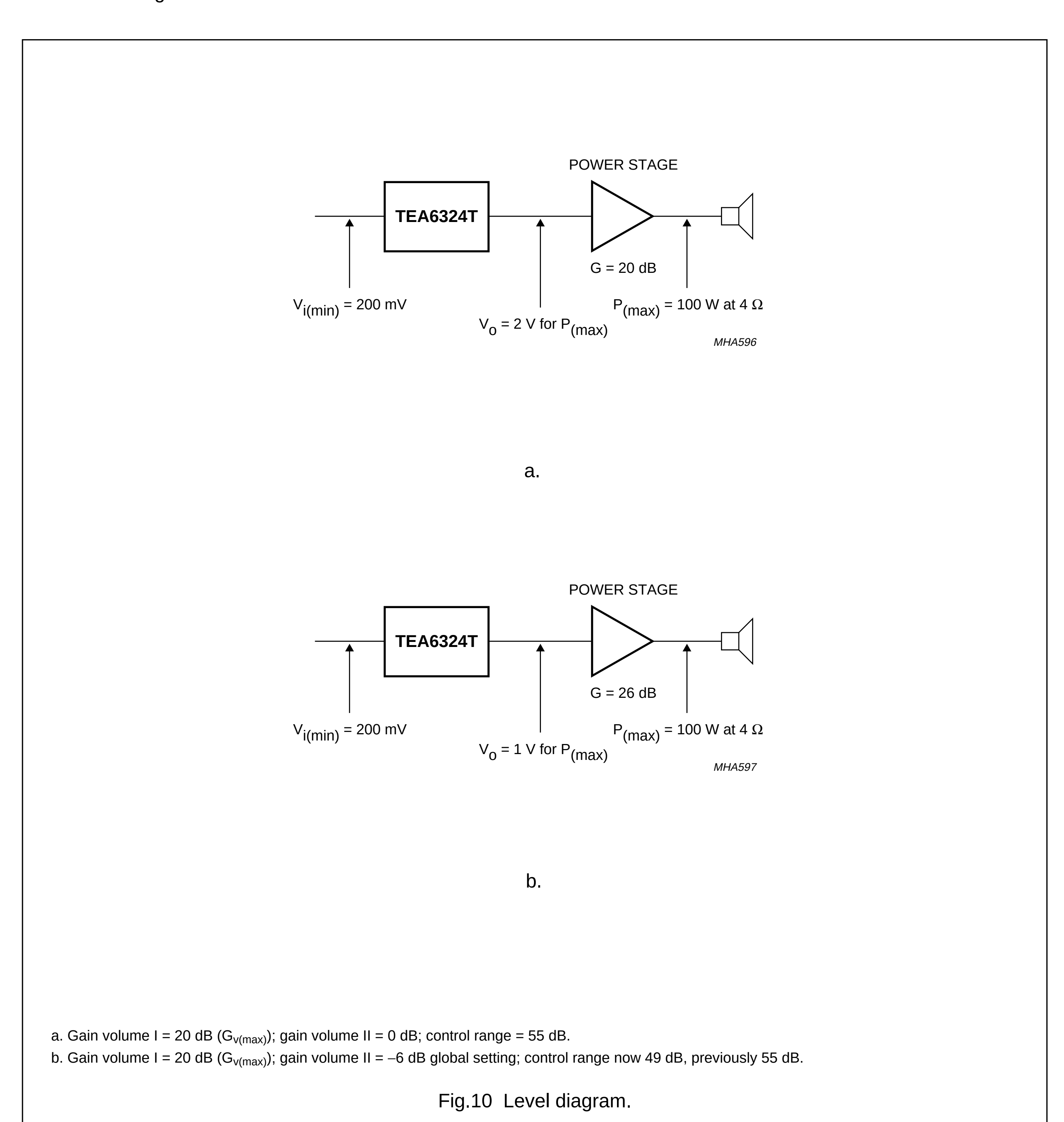


(1) Typically 2.2 V; referenced to 3 × V_{BE}.

(2) Typically 1.5 V; referenced to 2 × V_{BE}.

Fig.9 Mute function diagram.

In cases where at the maximum volume position the 20 dB gain is not needed, it is recommended that the maximum boost gain should be used. This coupled with increased attenuation in the last section (volume II), results in a lower noise and offset voltage.



a. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = 0 dB; control range = 55 dB.
b. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = –6 dB global setting; control range now 49 dB, previously 55 dB.

Fig.10 Level diagram.

V_P
+8.5 V to oscilloscope
V_{CC} 8.5 V
4.7 kΩ
470 μF
inputs
TEA6324T
13 11 14 10 12
23
3 22
2 15 16
outputs to oscilloscope
5 × 220 nF
5 × 600 Ω
47 μF
100 μF
2 × 4.7 μF
2 × 10 kΩ
MHA598

Fig.11 Turn-on/off power supply circuit diagram.

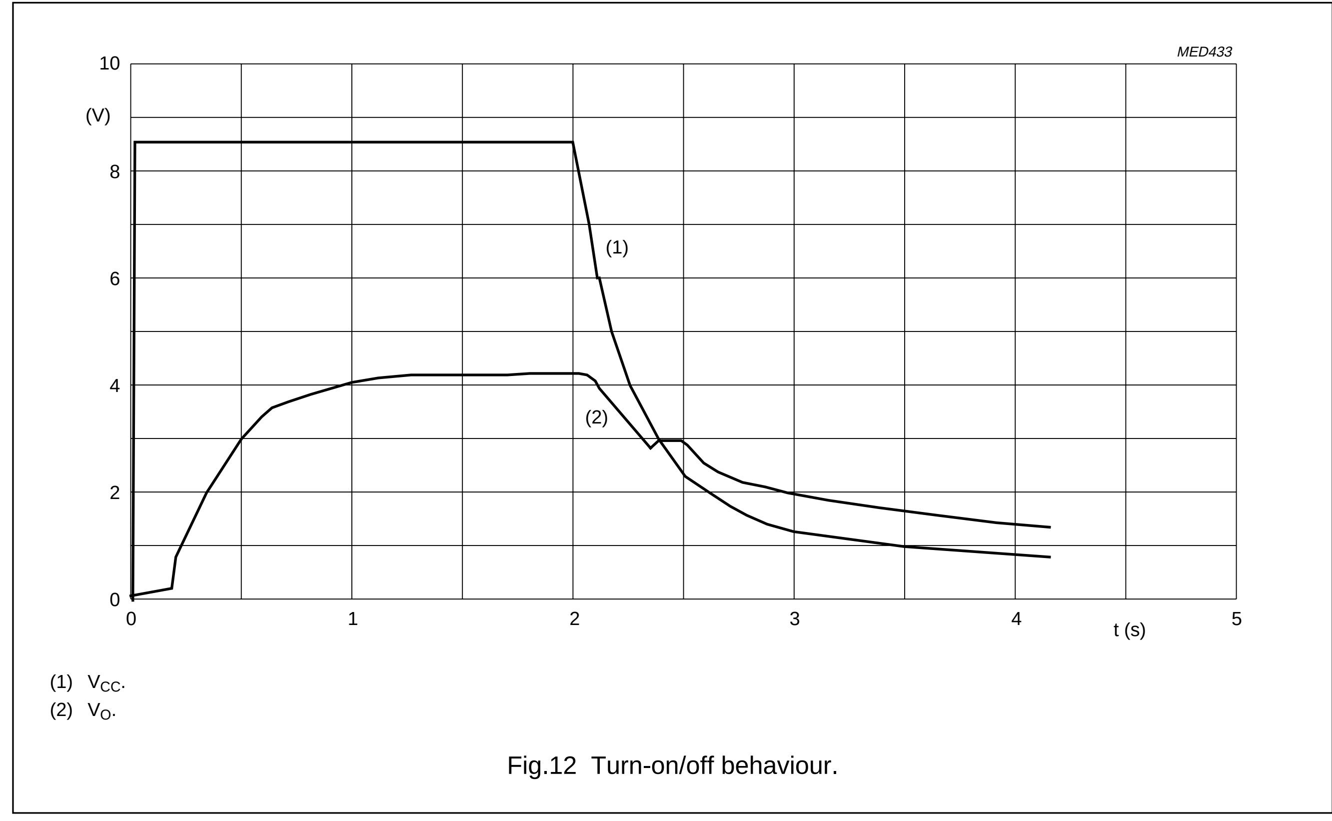


Fig.12 Turn-on/off behaviour.

3.4 kΩ
220 nF
270 nF
270 nF
5.6 nF
10 nF
100 μF
8 7 6 5 4 9
16
24 SCL
V_{CC} = 8.5 V
23
0.1 μF
TEA6324T
1 SDA
10 kΩ
2
1000 μF
47 μF
15
4.7 μF
output right
output left
V_P
0.2 V (RMS)
V_O
600 Ω
220 nF
input A and B
left and right
and input mono
17 18 19 20 21
MHA599
5.6 nF
220 nF
270 nF
270 nF
3.4 kΩ

Fig.13 Test circuit for power supply ripple rejection (RR).

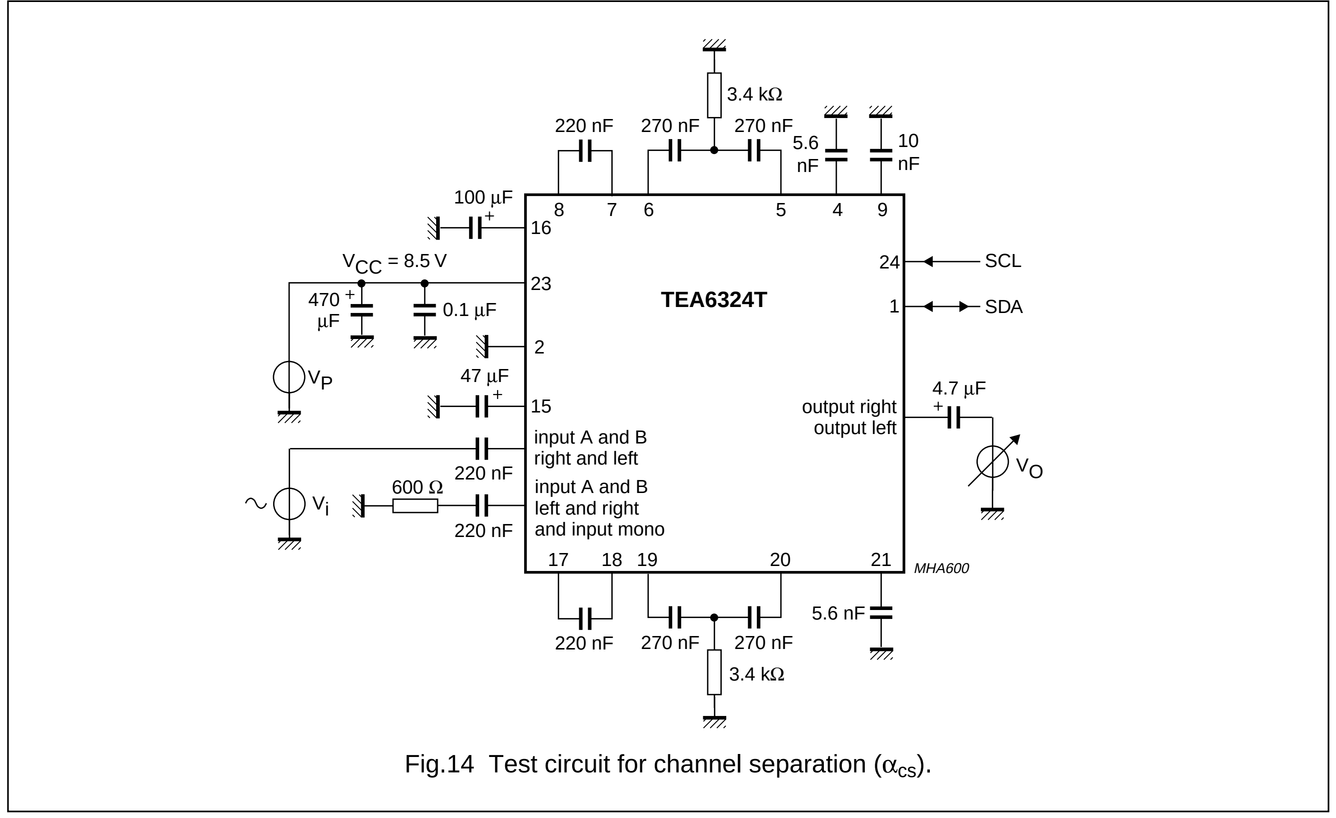


Fig.14 Test circuit for channel separation (α_{cs}).

Selection of input signals by using the zero crossing mute mode

The zero cross mute mode provides for a selection of input sources (A and B) for both left and right channels.
The following example (see Fig.15), shows a typical selection for the left input source signals IAL and IBL.
The initial selection of these channels produces a modulation click. The click is determined by the difference of the signal values at the time of switching.

At t_1 the maximum possible difference between signals is 7 V (p-p) (see Fig.15) and gives a large click. Using the cross detector no modulation click is audible.

With the selection enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I^2C-bus. The output signal follows the input A signal from –4 V, until the next zero crossing occurs and then activates mute.

After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal up to 3 V.

With a delay time of 40 ms ($t_2 – t_1$), the external capacitor C_m = 3.3 nF. This results with the zero cross function operating at the lowest frequency of 40 Hz determined by the C_m capacitor.

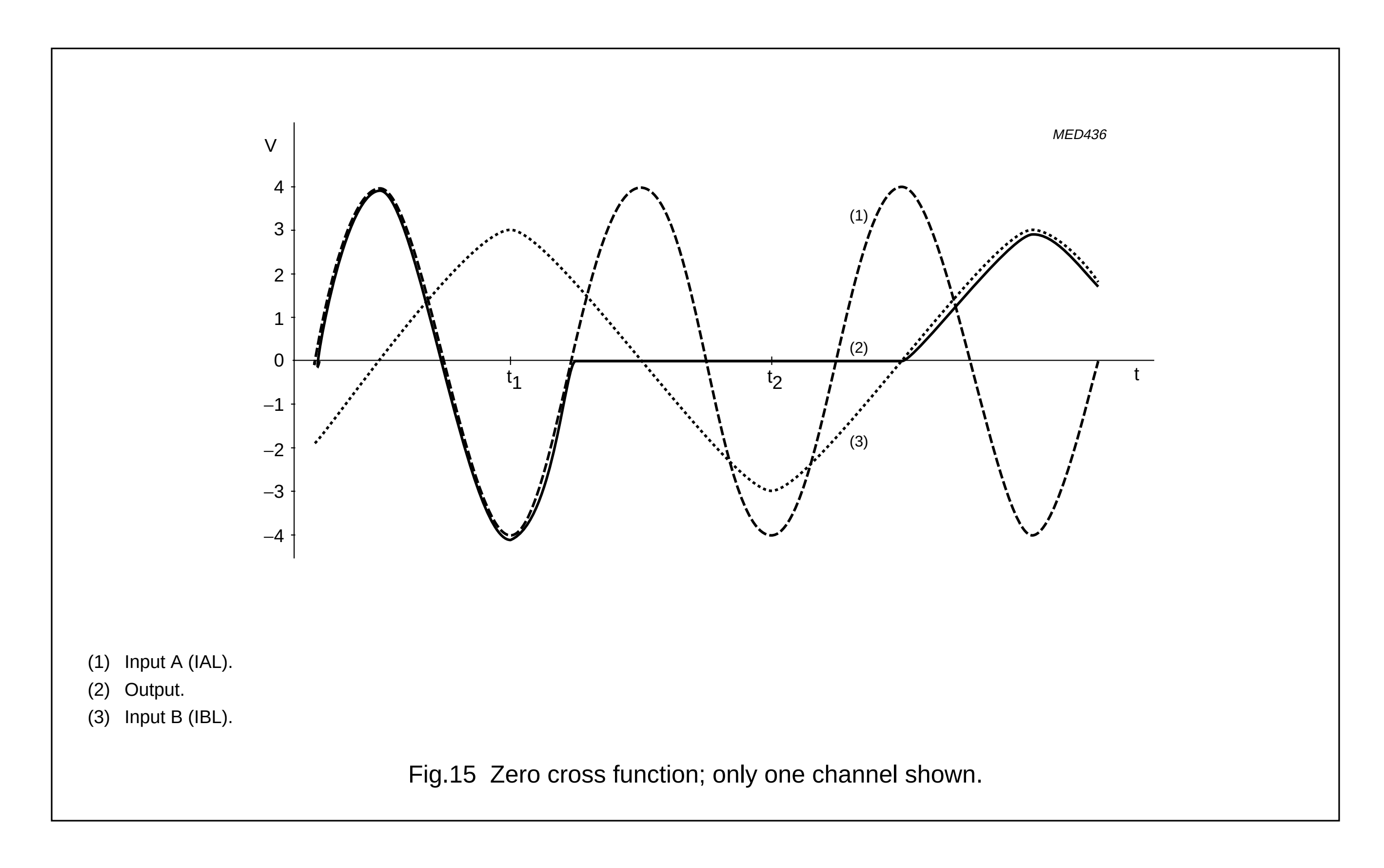


Fig.15 Zero cross function; only one channel shown.

INTERNAL PIN CONFIGURATIONS

Values shown in Figs 16 to 27 are typical DC values; V_{CC} = 8.5 V.

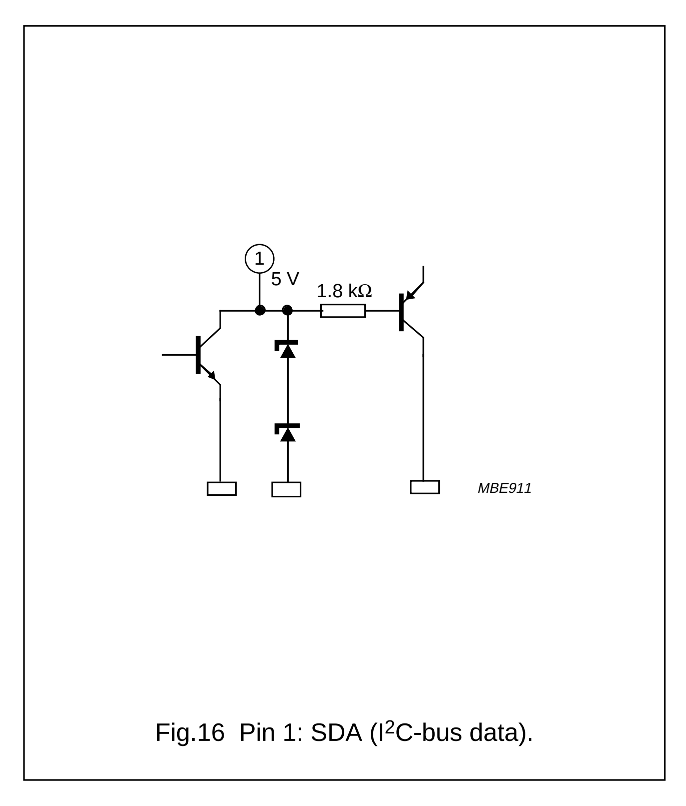


Fig.16 Pin 1: SDA (I^2C-bus data).

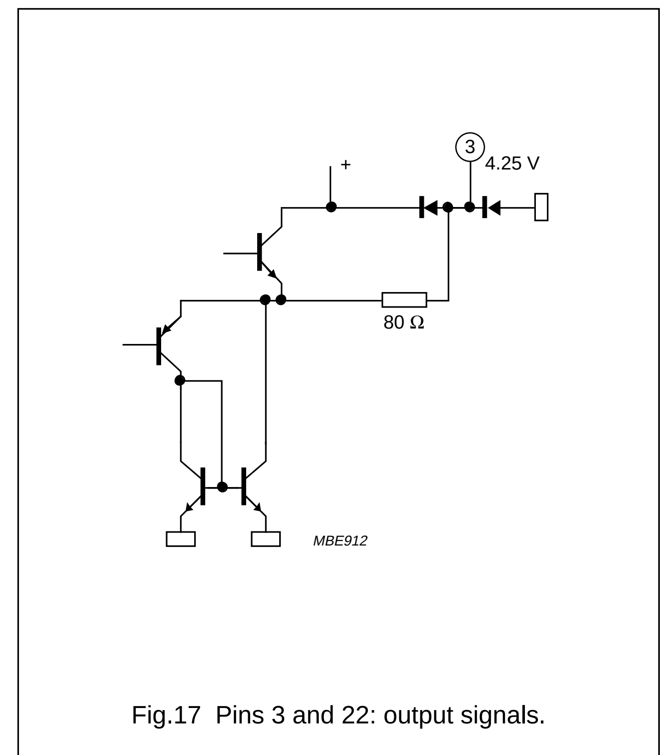


Fig.17 Pins 3 and 22: output signals.

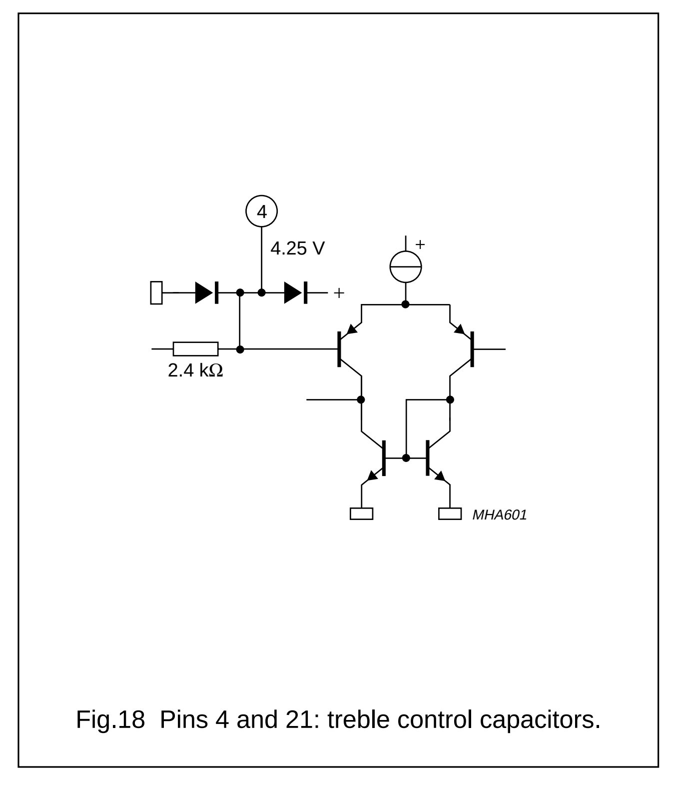


Fig.18 Pins 4 and 21: treble control capacitors.

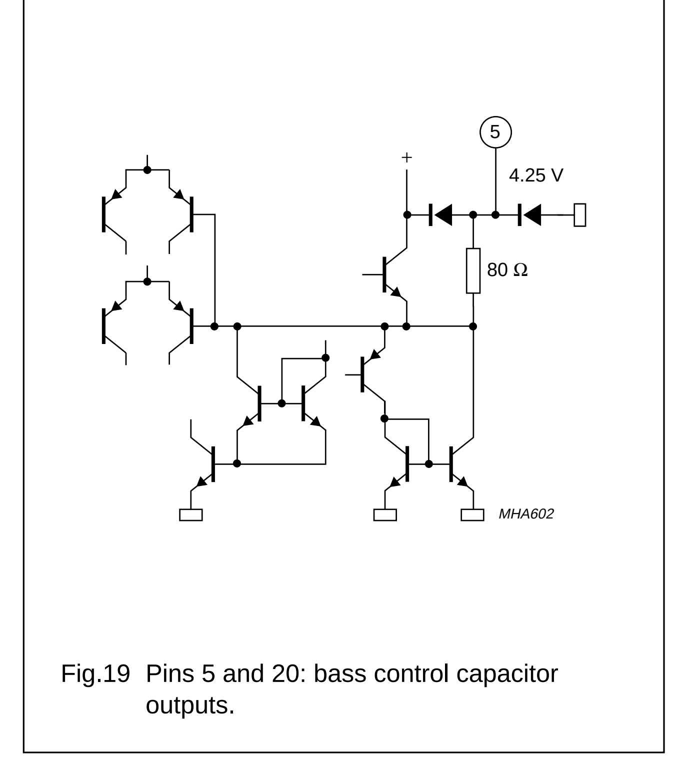


Fig.19 Pins 5 and 20: bass control capacitor outputs.

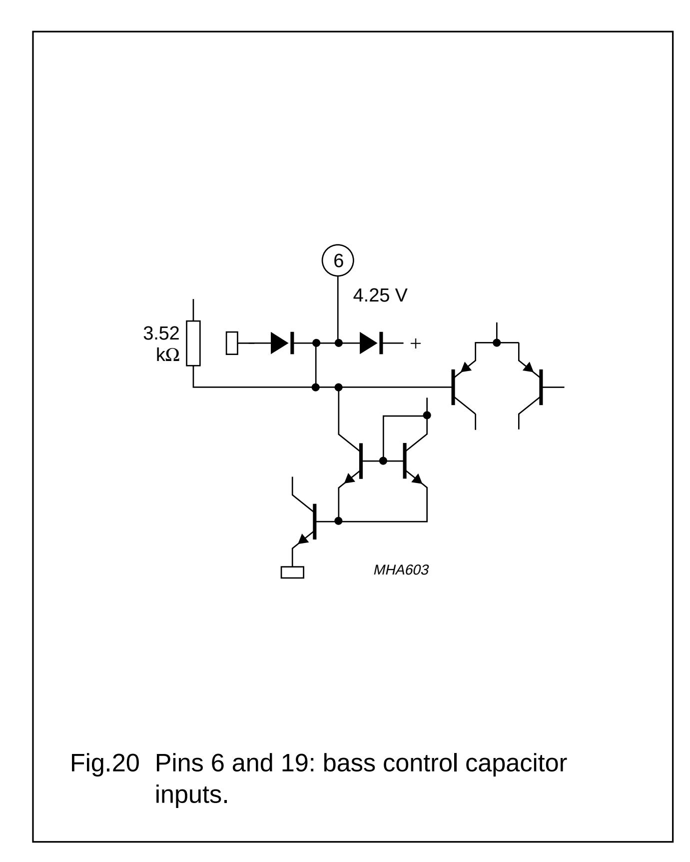


Fig.20 Pins 6 and 19: bass control capacitor inputs.

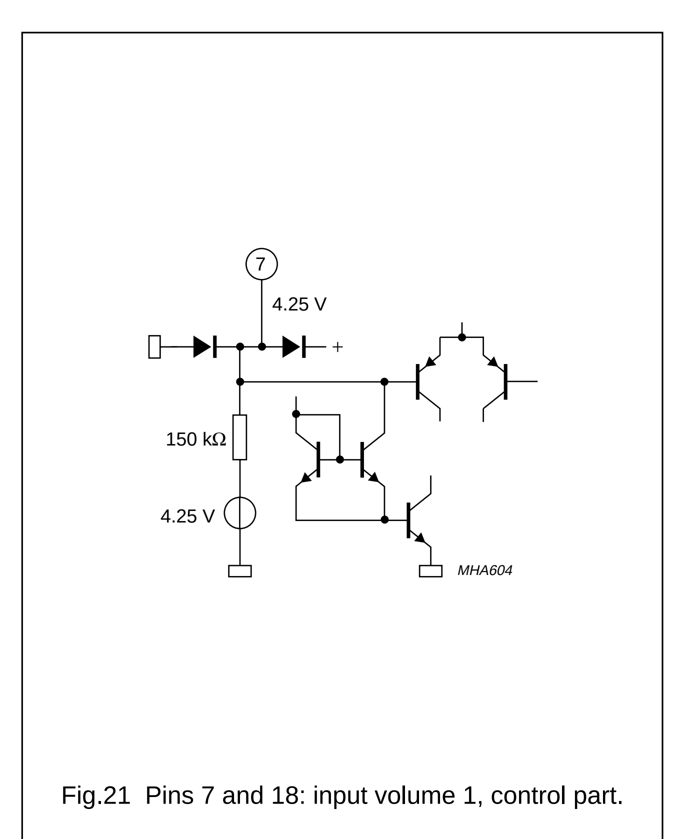


Fig.21 Pins 7 and 18: input volume 1, control part.

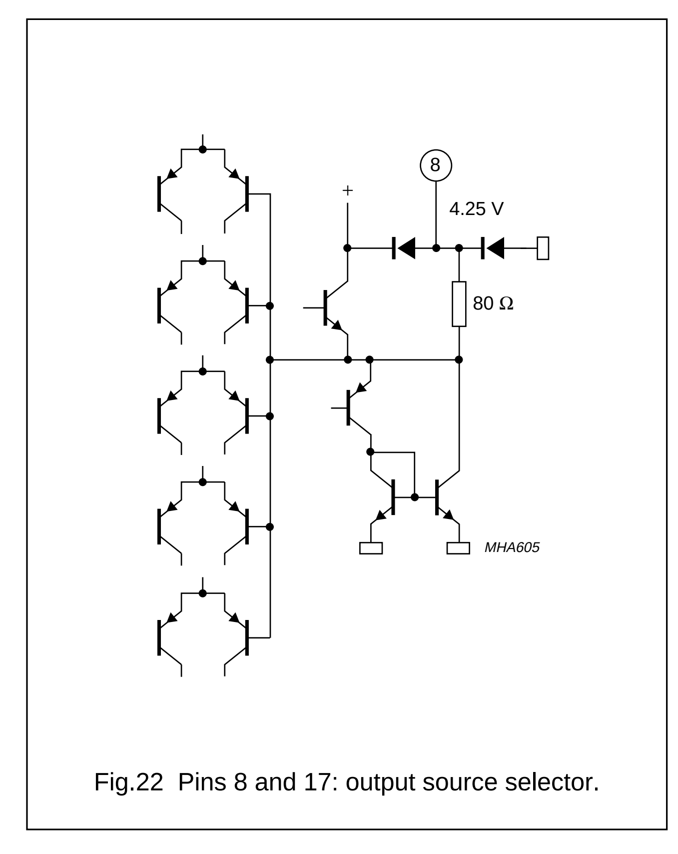


Fig.22 Pins 8 and 17: output source selector.

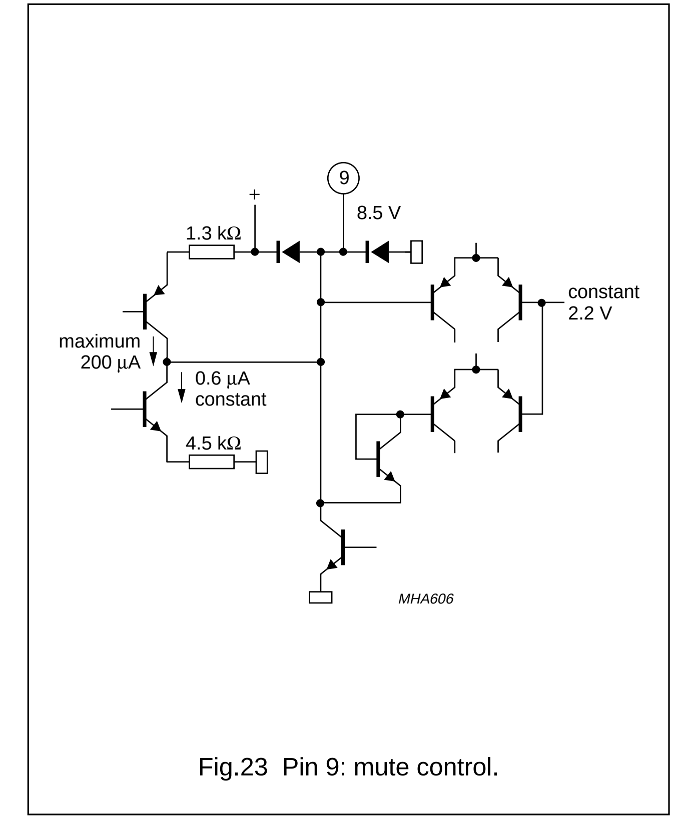


Fig.23 Pin 9: mute control.

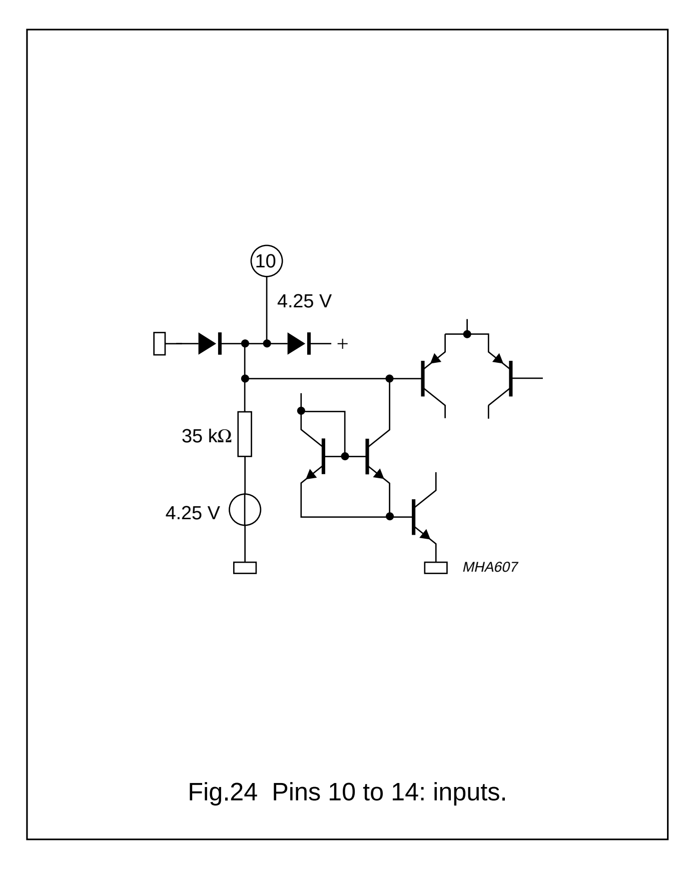


Fig.24 Pins 10 to 14: inputs.

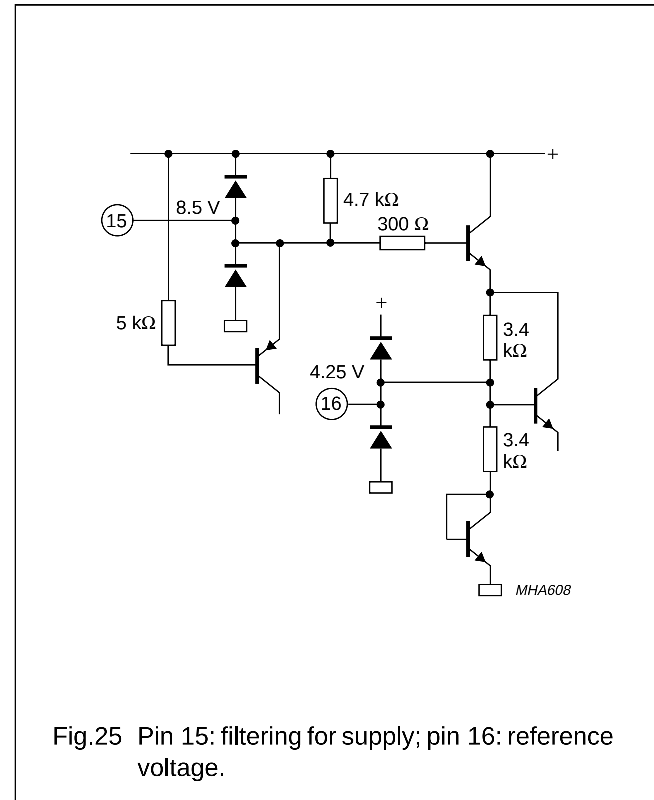


Fig.25 Pin 15: filtering for supply; pin 16: reference voltage.

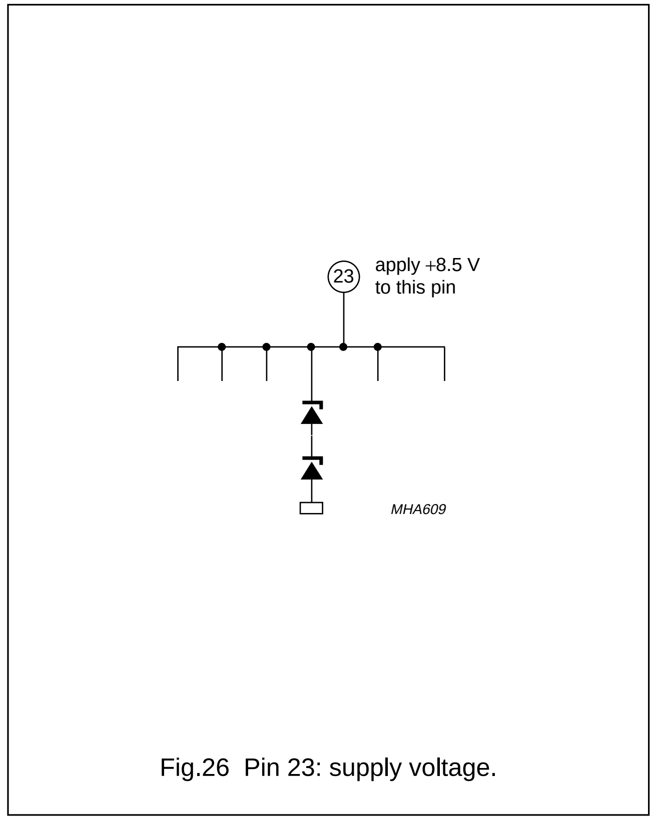


Fig.26 Pin 23: supply voltage.

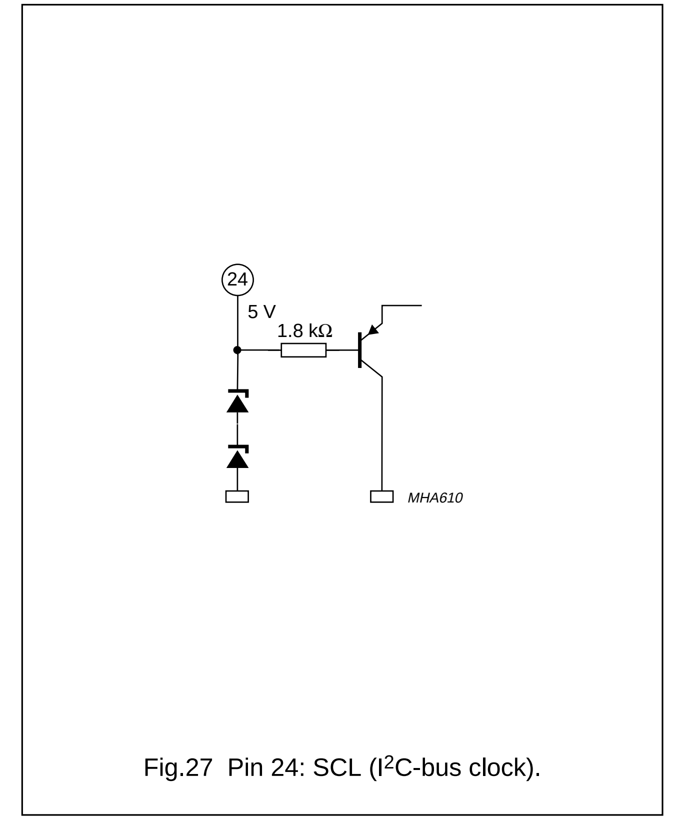
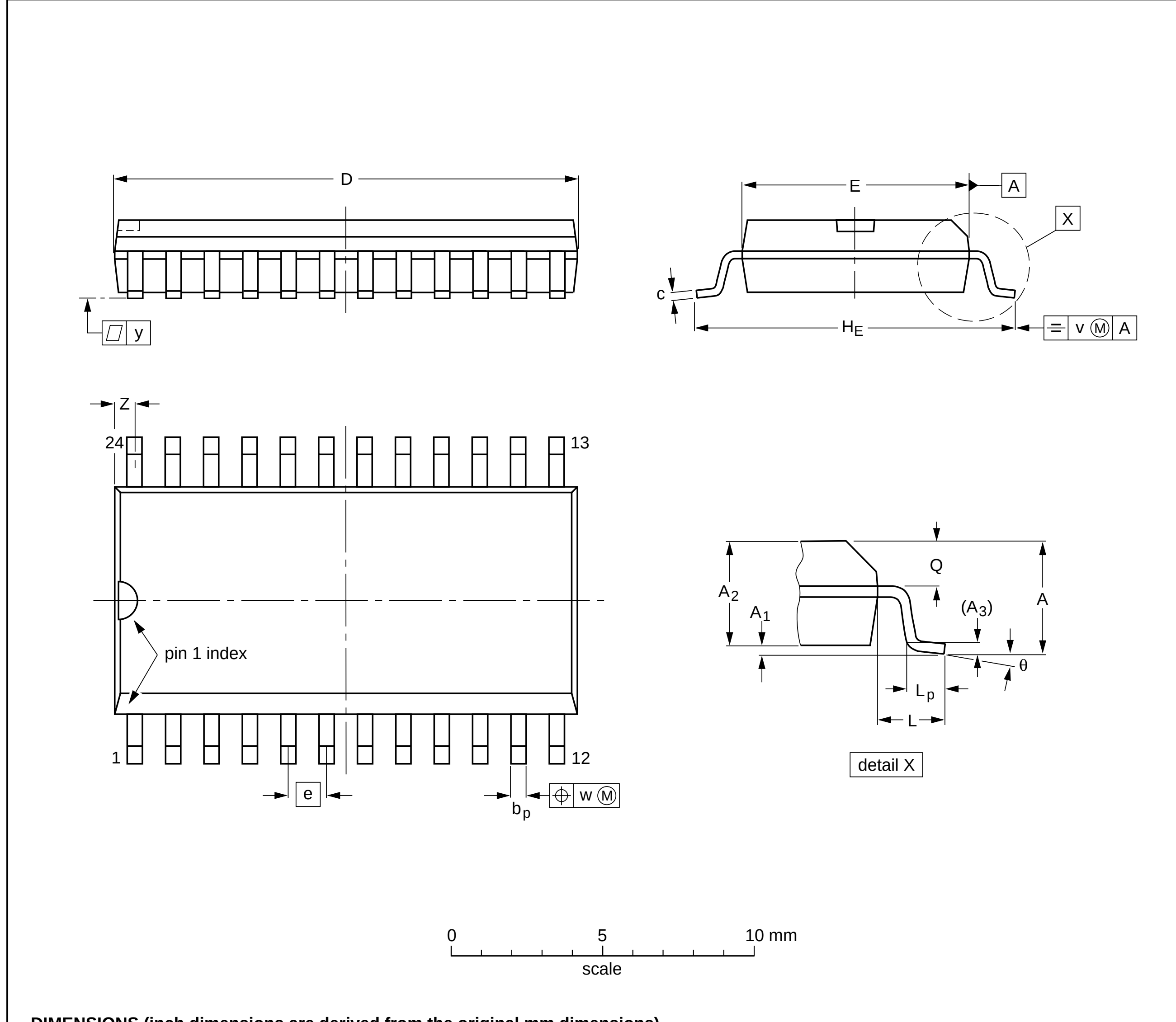


Fig.27 Pin 24: SCL (I^2C-bus clock).

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

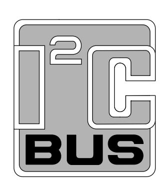
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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